

DATASHEET

DMT3N4R2U224M3DTA0

4.2V, 220mF, 300mΩ, -40°C to +85°C

Revision 3.0, March 2025



Electrical Specifications

Table 1: Absolute Maximum Ratings

Parameter	Name	Conditions	Min	Typical	Max	Units
Terminal Voltage	V_{peak}				4.2	V
Temperature	T_{max}		-40		+85	°C

Table 2: Electrical Characteristics

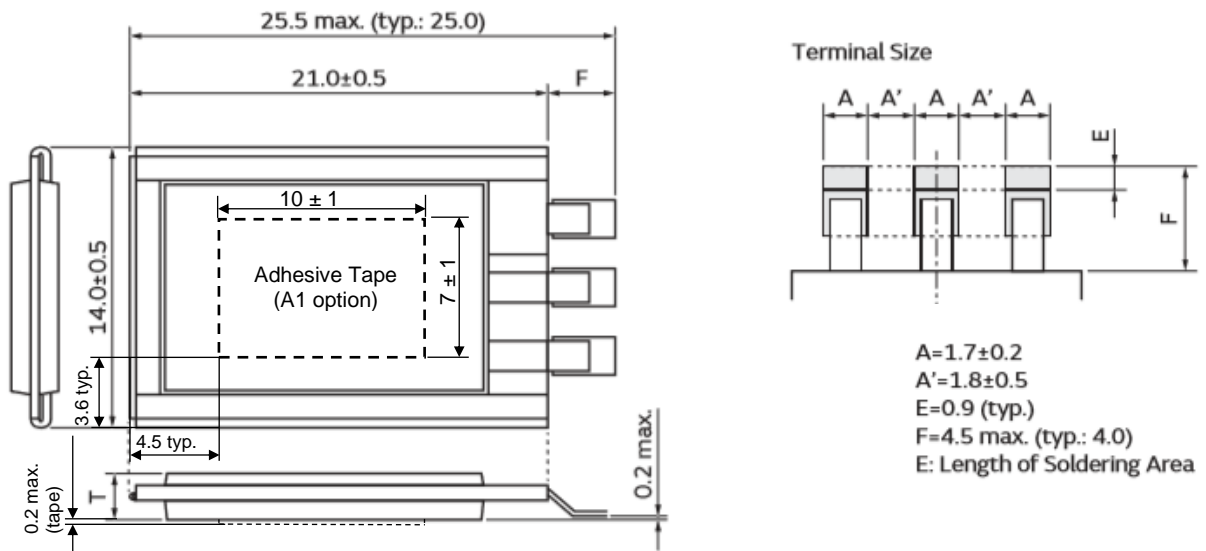
Parameter	Name	Conditions	Min	Typical	Max	Units
Terminal Voltage	V_n		0		4.2	V
Capacitance	C	DC, 23°C	176	220	264	mF
ESR	ESR	AC, 1kHz		300	360	mΩ
Leakage Current	I_L	4.2V, 23°C 120hrs		5	10	μA
RMS Current	I_{RMS}	25°C			3.2	A
Peak Current ¹	I_P	23°C			10	A

¹Non-repetitive current, single pulse to discharge fully charged supercapacitor.

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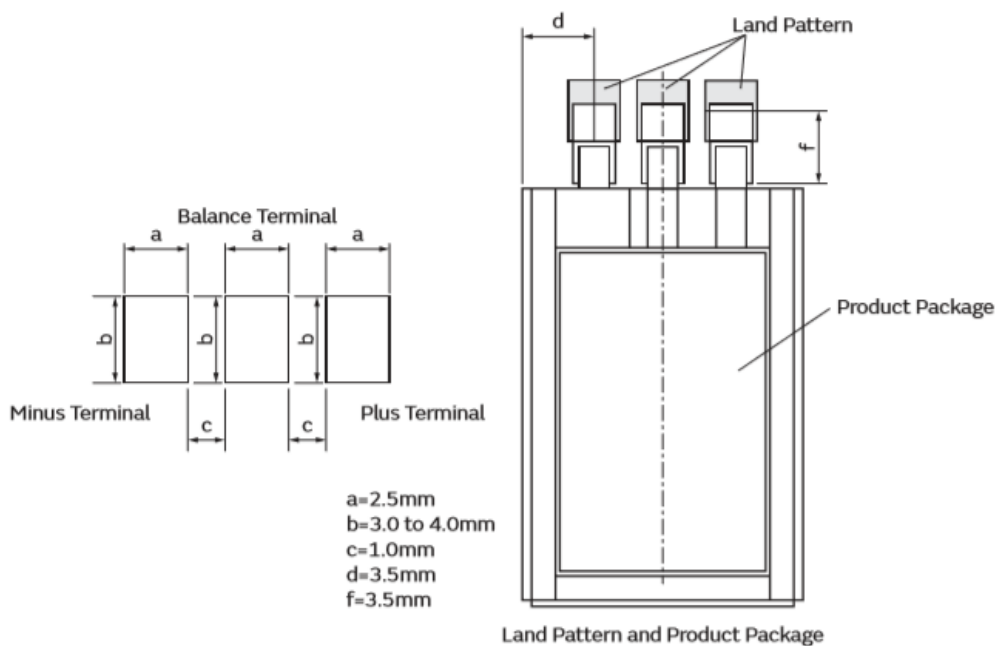
Table 3: Mechanical specification

	Length (mm)	Width (mm)	Thickness "T" (mm)	Weight (gm)
DMT3N4R2U224M3DTA0	21 ± 0.5mm	14 ± 0.5	2.2 (max. 2.5)	0.6
DMT3N4R2U224M3DTA1 (with adhesive tape on underside)	21 ± 0.5mm	14 ± 0.5	2.4 (max. 2.7)	0.6



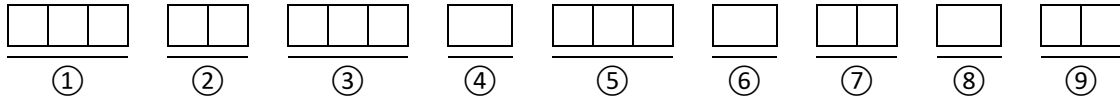
Mechanical drawing for DMT3N4R2U224M3DTA0

Landing Pad Dimensions



DMT3N4R2U224M3DTA0 DATASHEET

Part Numbering



① Series

Code	
DMT	General Purpose Type

② External Dimensions (L x W x T)

Code	L (mm)	W (mm)	T (mm)
33	21.0±0.5	14.0±0.5	3.5 (max 3.8)
4N	21.0±0.5	14.0±0.5	2.2 (max 2.5)

③ Rated Voltage

Code	Rated Voltage
4R2	DC 4.2V

④ ESR

Code	ESR @ 1kHz
S	130mΩ
U	300mΩ

⑤ Nominal Capacitance

First two are significant digits and the third expresses the number of zeroes which follow the two numbers

Code	Nominal Capacitance
224	22x10 ⁴ μF = 220mF

⑥ Capacitance Tolerance

Code	Tolerance
M	±20%

⑦ External Terminal

Code	Terminal Specification
3D	3 Terminals (+/-/Balance)

⑧ Packaging

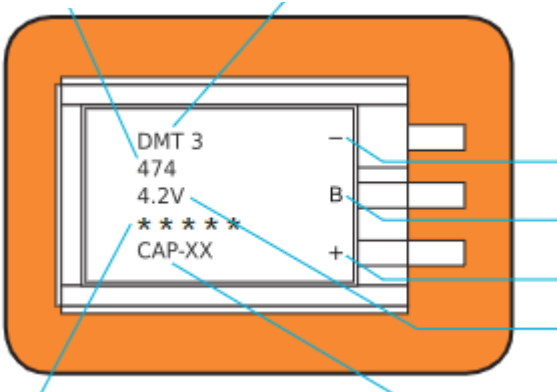
Code	Package Specification
T	Tray type, 50pcs/Tray

⑨ Inhouse Specification Code

Expressed by two-digit alphanumerics

Printing

Capacitance Series Code + LW Size Code



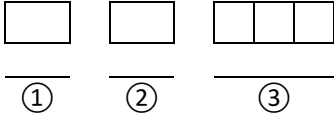
Negative Terminal
Balance Terminal
Positive Terminal
Rated Voltage

Batch ID

Manufacturer (CAP-XX or MURATA)

DMT3N4R2U224M3DTA0 DATASHEET

Batch ID



① Year

Code	Year
9	2019
A	2020
B	2021
C	2022
D	2023
:	:
Y	2044
Z	2045

② Month

Code	Month
F	January
G	February
H	March
J	April
K	May
L	June
M	July
N	August
P	September
Q	October
R	November
S	December

③ 3-digit Unique ID

The following code is used to identify the batch within the month

Definition of Terms

In its simplest form, the Equivalent Series Resistance (ESR) of a capacitor is the real part of the complex impedance. In the time domain, it can be found by applying a step discharge current to a charged cell as in Fig. 1. In this figure, the supercapacitor is pre-charged and then discharged with a current pulse, $I = 1A$ for duration 0.01 sec.

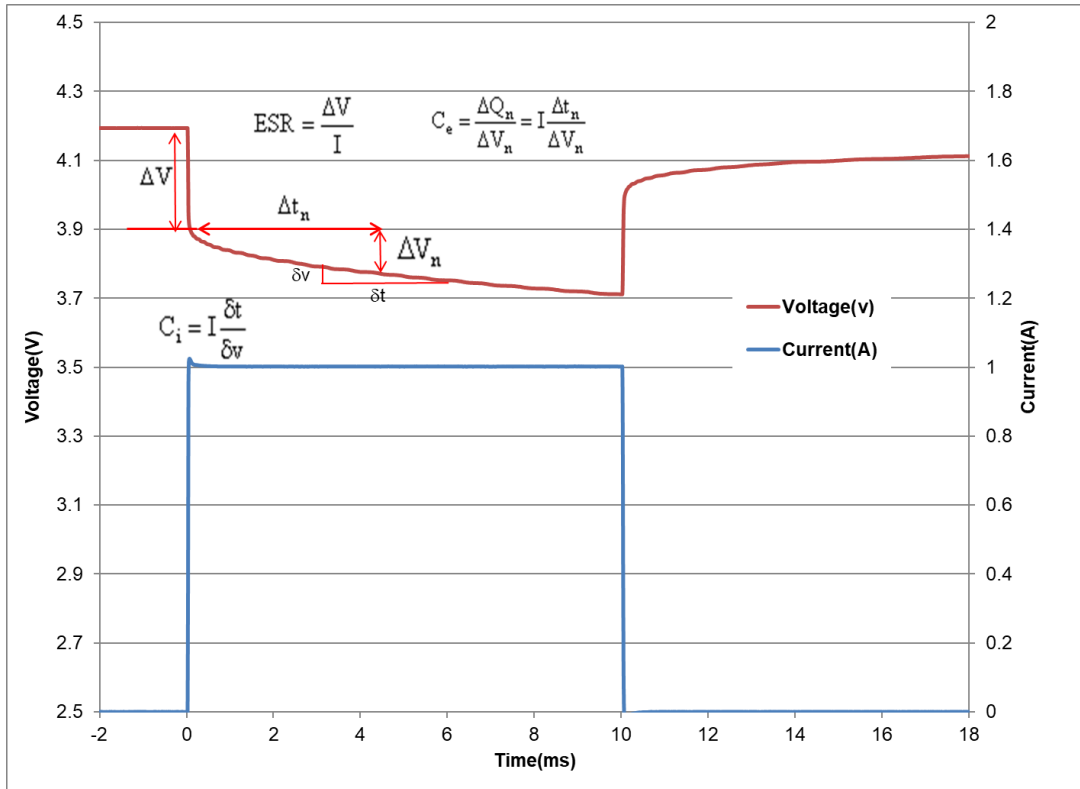


Fig 1: Effective capacitance, instantaneous capacitance and ESR for an DMT3N4R2U224M3DTA0

The ESR is found by dividing the instantaneous voltage step (ΔV) by I . In this example = $(4.194V - 3.921V)/1A = 273m\Omega$.

The instantaneous capacitance (C_i) can be found by taking the inverse of the derivative of the voltage, and multiplying it by I .

The effective capacitance for a pulse of duration Δt_n , $C_e(\Delta t_n)$ is found by dividing the total charge removed from the capacitor (ΔQ_n) by the voltage lost by the capacitor (ΔV_n). For constant current $C_e(\Delta t_n) = I \times \Delta t_n / \Delta V_n$. C_e increases as the pulse width increases and tends to the DC capacitance value as the pulse width becomes very long (~10 secs). After 2msecs, Fig 1 shows the voltage drop $V_{2ms} = (3.921 V - 3.811V) = 110mV$. Therefore $C_e(2ms) = 1A \times 2ms / 110mV = 18.2mF$. After 10ms, the voltage drop = $3.921 V - 3.711V = 210mV$. Therefore $C_e(10ms) = 1 A \times 10ms / 210mV = 47.6mF$. The DC capacitance of a DMT3N4R2U224M3DTA0 = 0.22 F. Note that ΔV , or $I \times R$ drop, is not included because very little charge is removed from the capacitor during this time. C_e shows the time response of the capacitor and it is useful for predicting circuit behaviour in pulsed applications.

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Measurement of DC Capacitance

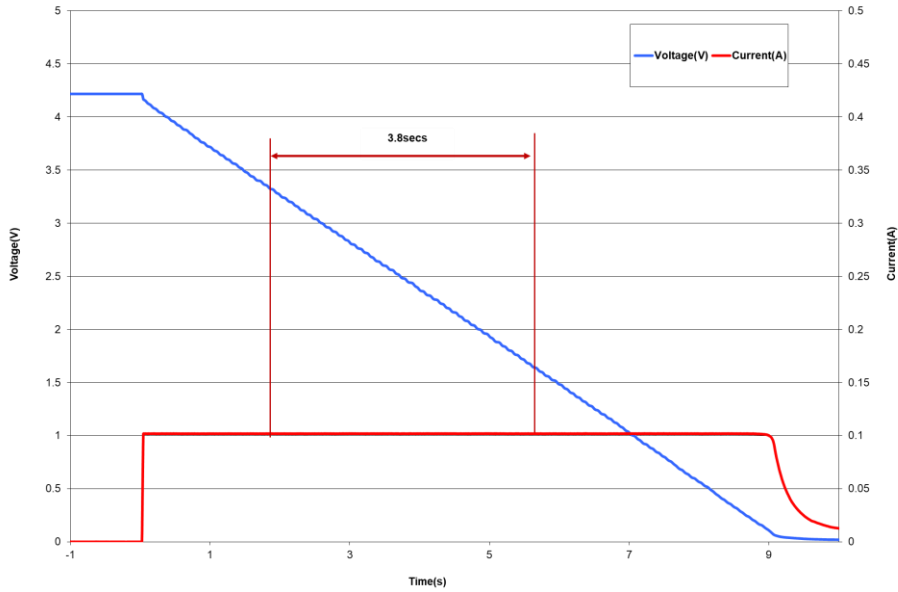


Fig 2: Measurement of DC Capacitance for a DMT3N4R2U224M3DTA0

Fig 2 shows the measurement of DC capacitance by drawing a constant 100mA current from a fully charged supercapacitor and measuring the time taken to discharge from 80% to 40% of V_{rated} . In this case, $C = 0.1A \times 3.8s / (3.36-1.68)V = 226mF$, which is well within the 220mF +/- 20% tolerance for a DMT3N4R2U224M3DTA0 cell.

Measurement of ESR

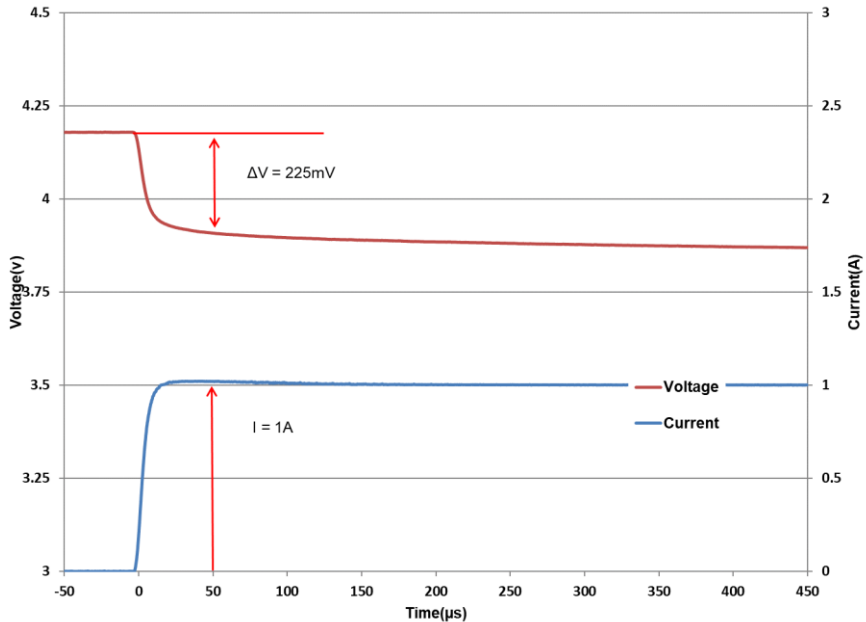


Fig 3: Measurement of ESR for a DMT3N4R2U224M3DTA0

Fig 3 shows DC measurement of ESR by applying a step load current to the supercapacitor and measuring the resulting voltage drop. CAP-XX waits for a delay of 50μs after the step current is applied to ensure the voltage and current have settled. In this case the ESR is measured as $225mV/1A = 225m\Omega$.

Effective Capacitance

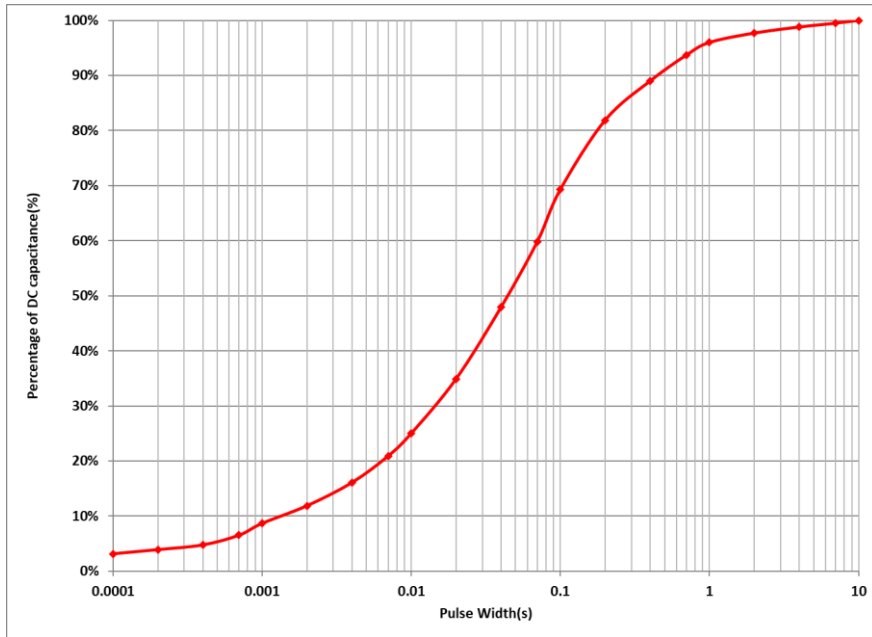


Fig 4: Effective Capacitance

Fig 4 shows the effective capacitance for the DMT3N4R2U224M3DTA0 @ 23°C. This shows that for a 1msec PW, you will measure 9% of DC capacitance or 20mF. At 10msecs you will measure 25% of the DC capacitance, and at 100msecs you will measure 69% of DC capacitance. Effective is a time domain representation of the supercapacitor's frequency response. If, for example, you were calculating the voltage drop if the supercapacitor was supporting 1A for 10msecs, then you would use the $C_{eff}(10msecs) = 25\%$ of DC capacitance = 55mF for a DMT3N4R2U224M3DTA0 , so $V_{drop} = 1A \times ESR + 1A \times duration/C = 1A \times 300m\Omega + 1A \times 10ms / 55mF = 482mV$.

Pulse Response

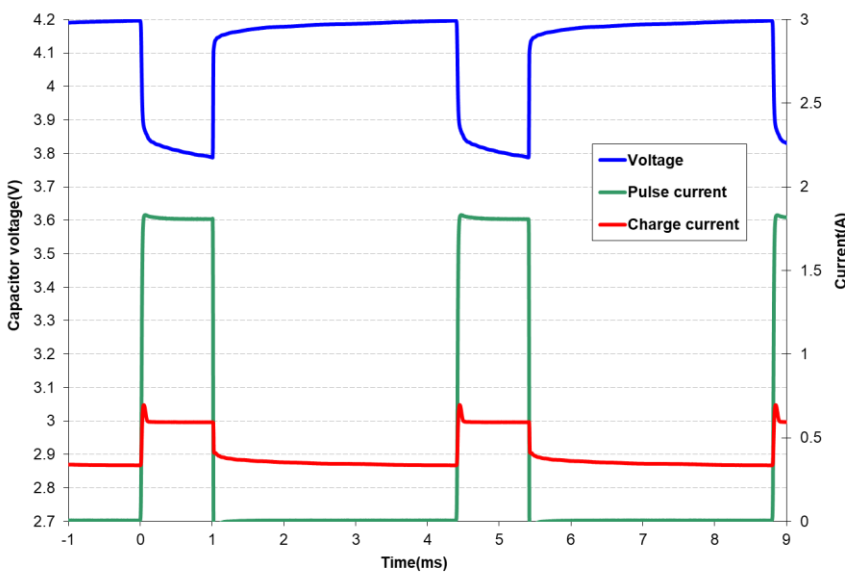


Fig 5 shows that the DMT3N4R2U224M3DTA0 supercapacitor does an excellent job supporting a GPRS class 10 pulse train, drawing 1.8A for 1.1ms at 25% duty cycle. The source is current limited to 0.6A and the supercapacitor provides the 1.2A difference to achieve the peak current. At first glance the freq response of Fig 8 indicates the supercapacitor would not support a 1ms pulse, but the C_{eff} of 20mF coupled with the low ESR supports this pulse train with only ~410mV droop in the supply rail.

Fig 5: DMT3N4R2U224M3DTA0 Pulse Response with GPRS Class 10 Pulse Train

DC Capacitance variation with temperature

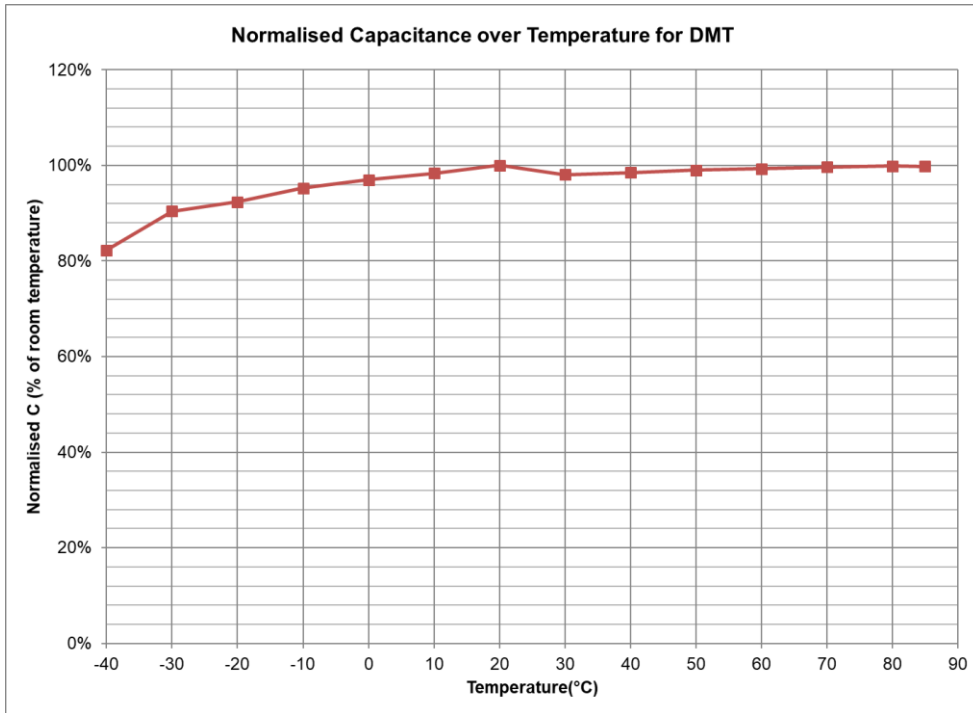


Fig 6: Capacitance change with temperature

Fig 6 shows that DC capacitance is approximately constant with temperature to 0°C and then at -40°C reduces to ~80% of DC capacitance at room temperature.

ESR variation with temperature

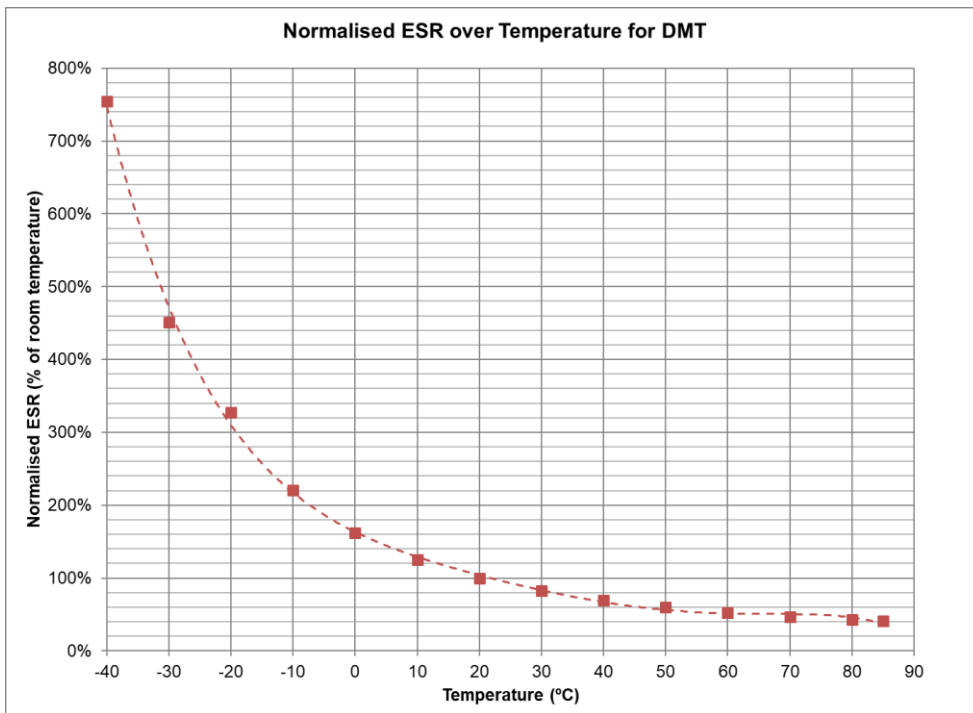


Fig 7: ESR change with temperature

Fig 7 shows that ESR at -40°C is ~7.5 x ESR at room temp, and that ESR at 70°C is ~0.5 x ESR at room temperature.

Frequency Response

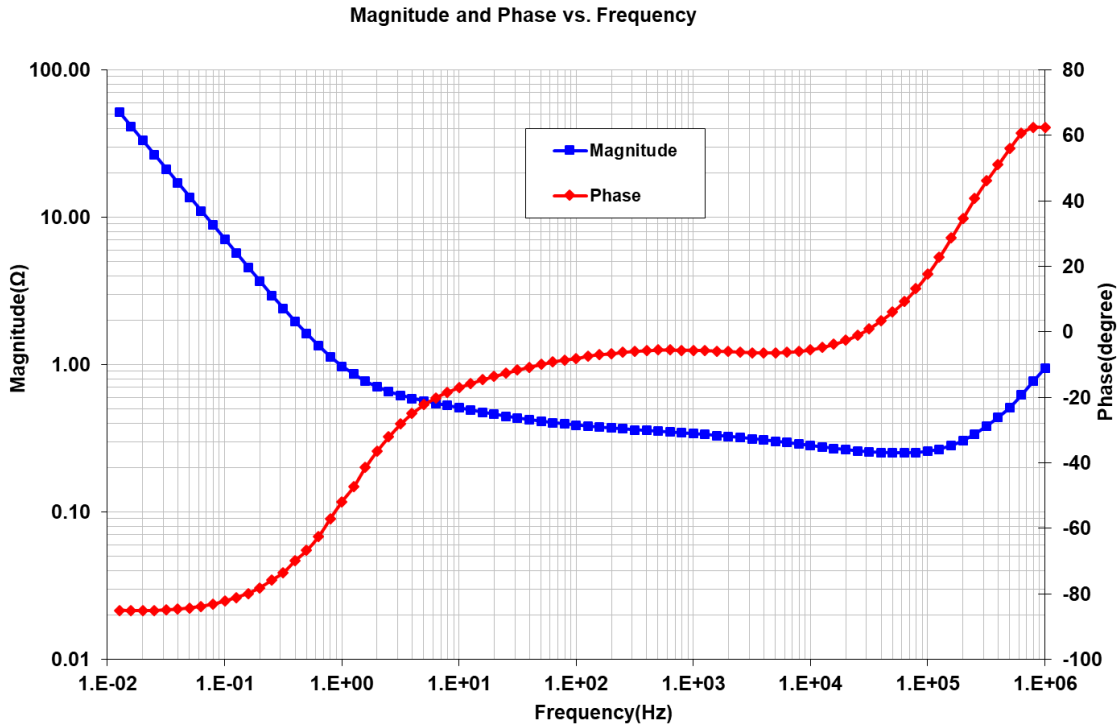


Fig 8: Frequency Response of Impedance (biased at 4.2V with a 50mV test signal)

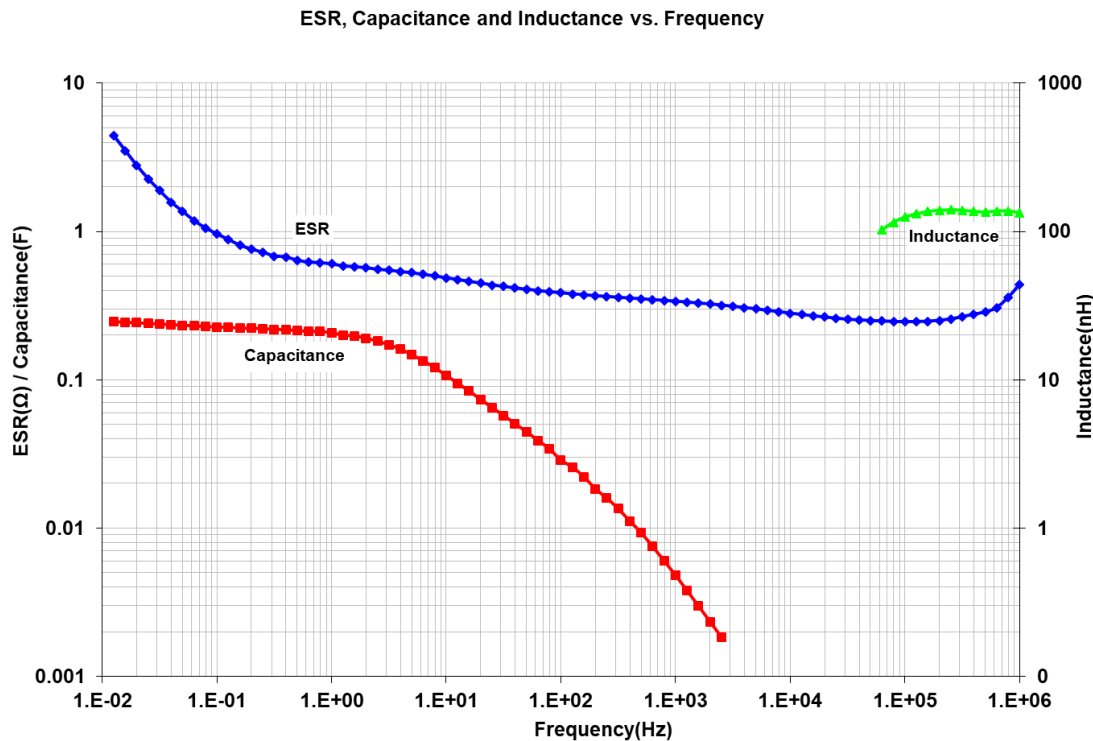


Fig 9: Frequency Response of ESR, Capacitance & Inductance

Fig 8 shows the supercapacitor behaves as an ideal capacitor until approx. 1.25 Hz when the magnitude no longer rolls off proportionally to $1/\text{freq}$ and the phase crosses -45° . Performance of supercapacitors with frequency is complex and the best predictor of performance is Fig 4 showing effective capacitance as a function of pulse width.

Leakage Current

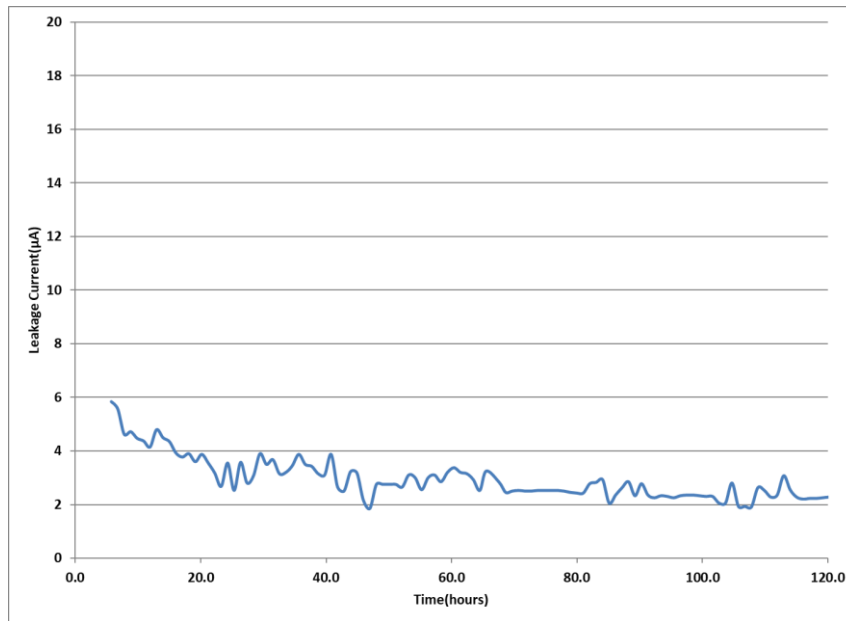


Fig 10: Leakage Current

Fig 10 shows the leakage current for DMT at room temperature. The leakage current decays over time, and the equilibrium value leakage current will be reached after ~120hrs at room temperature. The typical equilibrium leakage current is 2µA at room temperature.

Charge Current

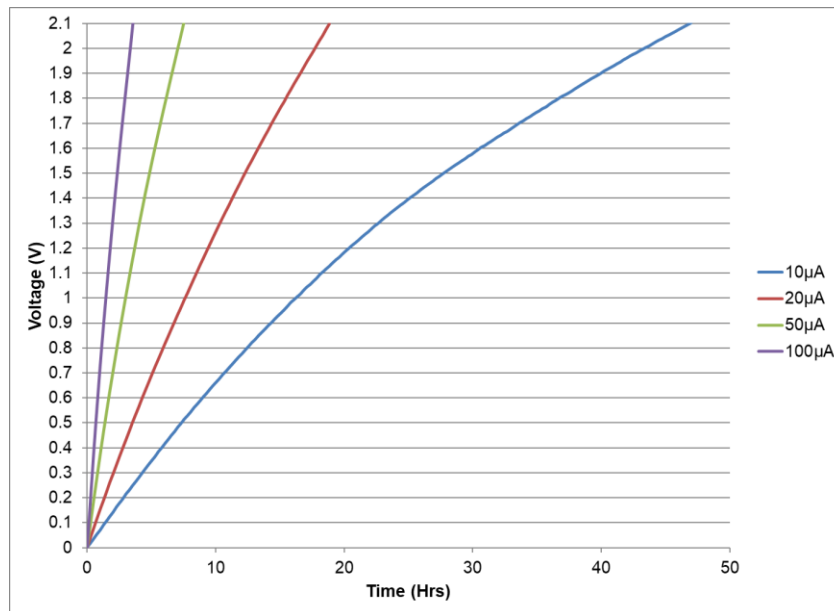


Fig 11: Charging a single cell of DMT3N4R2U224M3DTA0 (single cell: 440mF) with low current

The corollary to the slow decay in leakage currents shown in Fig 10 is that charging a supercapacitor at very low currents takes longer than theory predicts. At higher charge currents, the charge rate is as theory predicts. For example, it should take $0.44F \times 2.1V / 0.00002A = 12.8hrs$ to charge a 0.44 F supercapacitor to 2.1V at 20µA, but Fig 11 shows it took 19hrs. At 100µA charging occurs at a rate close to the theoretical rate.

RMS Current

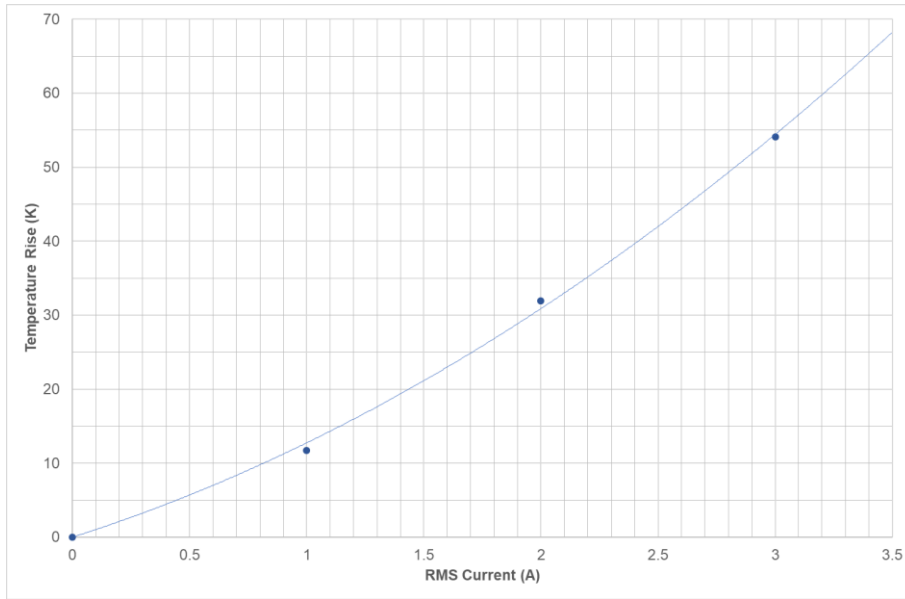


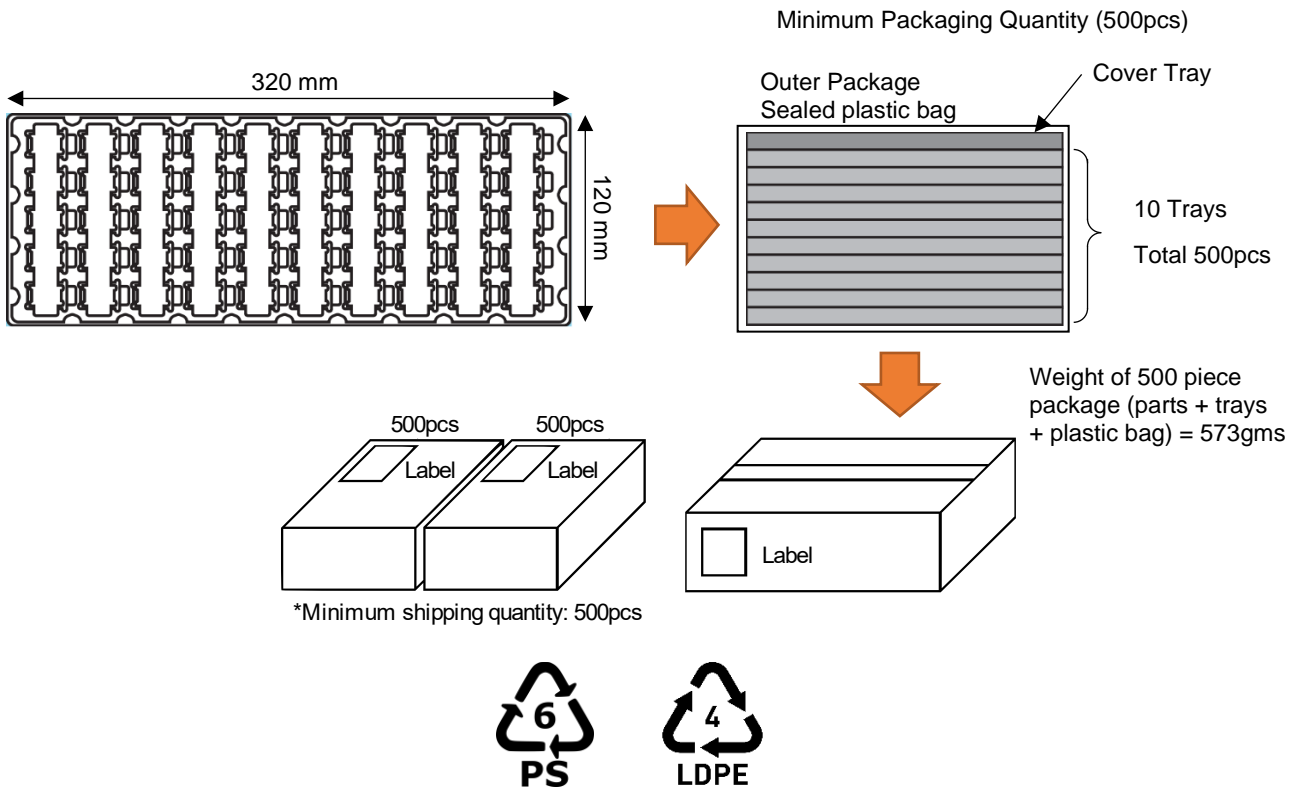
Fig 12: Temperature rise in DMT3N4R2U224M3DTA0 with RMS current

Continuous current flow into/out of the supercapacitor will cause self-heating, which limits the maximum continuous current the supercapacitor can handle. This is measured by a current square wave with 50% duty cycle, charging the supercapacitor to rated voltage at a constant current, then discharging the supercapacitor to half rated voltage at the same constant current value. For a square wave with 50% duty cycle, the RMS current is the same as the current amplitude. Fig 12 shows the increase in temperature as a function of RMS current. From this, the maximum RMS current in an application can be calculated, for example, if the ambient temperature is 40°C, and the maximum desired temperature for the supercapacitor is 85°C, then the maximum RMS current should be limited to 2.6A, which causes a 45°C temperature increase.

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Packaging

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CAP-XX uses sustainable packaging. All our packaging material are recyclable. The clear product trays are made from Polystyrene. ESD safe bubble wraps and bags are made from LDPE. The shipping boxes are corrugated cardboard. Please ensure all packaging is disposed in accordance with the relevant recycling procedures of the region where CAP-XX products are used.

Storage

CAP-XX recommends storing supercapacitors in their original packaging in an air-conditioned room ($\leq 25\text{ }^{\circ}\text{C}$) and $< 50\%$ relative humidity. Storage at continuous high temperature and humidity is not recommended and will cause premature ageing.

Do not store supercapacitors in the following environments:

- High temperature / high humidity
- Direct sunlight
- In direct contact with water, salt, oil or other chemicals
- In direct contact with corrosive materials, acids, alkalis or toxic gases
- Dusty environment
- In environments subjected to shock and vibration

Shelf Life

Supercapacitors have a shelf life of minimum 2 years when stored uncharged at recommended storage conditions.

Cautions before use

CAP-XX supercapacitors are “burned in” during production, and have a defined polarity, as shown by the positive terminal marked on the face of the product. Reversing the polarity of the device will not damage the device but may cause a rise in the ESR and will void the warranty. Please verify the orientation of the supercapacitor in accordance with the product markings before assembly.

CAP-XX supercapacitors are heat-sensitive. Over-heating of the supercapacitor may result in a degradation of performance and useful life.

CAP-XX supercapacitors must only be used within their rated voltage range. Over-voltage may cause swelling and eventually, product failure.

CAP-XX supercapacitors are fully discharged when shipped. Devices should be handled and soldered in a discharged state.

Soldering and Assembling

CAP-XX supercapacitors are designed for direct soldering onto the PCB. Soldering the terminals to the PCB will ensure the highest contact reliability and lowest contact resistance. Do NOT solder directly to the device casing. This will cause permanent internal damage to the supercapacitor.

CAP-XX supercapacitors are NOT SUITABLE for infrared reflow soldering, hot-air reflow soldering, or wave soldering. They should be mounted as a secondary operation, using a manual soldering iron, a hot bar soldering jig, conductive adhesive, ultrasonic welding or laser welding.

CAP-XX recommends the use of a water-soluble flux, or a no-clean (low residue) flux, and low temperature solder compounds.

Please solder under the following conditions:

- Solder Type: Resin flux cored solder wire ($\varnothing 1.2\text{mm}$)
- Solder: Lead-free solder: Sn-3Ag-0.5Cu
- Soldering iron temperature at $350^{\circ}\text{C}\pm 10^{\circ}\text{C}$
- Solder iron wattage: 70W or less
- Soldering time: 3 to 4sec.
- The same terminal should be soldered 3 or less times.

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If a hot-air gun is used to reflow the solder during a re-mount or de-mount, care must be taken to prevent excessive heating of the package adjacent to the solder terminals. Allow at least 15 sec between successive soldering attempts for the device to cool down.

Please consult CAP-XX if you wish to wash the device after soldering.

Vibration and Shock Testing

Shock

CAP-XX has undertaken tests in accordance with IEC68-2-27 to determine the effects of repeated shocks on both the mechanical integrity and electrical performance of its supercapacitors:

- Type: Half-Sine
- Amplitude: 30G
- Duration: 18ms
- No. of cycles: 3 in each direction (18 in total)
- No. of axes: 3, orthogonal

Results: final C \geq 80% of initial, final ESR \leq 120% of initial, the final thickness is within specification.

Note that this test was undertaken on the standard product with adhesive mounting tape (Nitto No.5000NS). To achieve the highest levels of resistance to shock, CAP-XX recommends the use of an adhesive mounting tape on the underside of the device.

Vibration

CAP-XX has undertaken tests to determine the effects of sustained vibration on both the mechanical integrity and electrical performance of its supercapacitors.

The test standard is in accordance with IEC60065-2-6.

- Type: Sinusoidal
- Frequency: 10 - 500Hz
- Amplitude: 0.75 mm or acceleration: 100 m/s² (whichever is less stringent)
- Sweep Rate: 1 min/octave
- No. of cycles: 10 (10Hz - 500Hz - 10Hz)
- No. of axes: 3, orthogonal
- Total test time: 6 hours

Results: final C \geq 80% of initial, final ESR \leq 120% of initial, the final thickness is within specification.

Note that this test was undertaken on the standard product with adhesive mounting tape (Nitto No.5000NS). To achieve the highest levels of resistance to shock, CAP-XX recommends the use of an adhesive mounting tape on the underside of the device.

Drop Test

CAP-XX has undertaken tests to determine the effects of repeated drops on both the mechanical integrity and electrical performance of its supercapacitors:

Supercapacitor is discharged

- Mount product to 150g box with adhesive mounting tape (Nitto No.5000NS)
- Drop the box from 0.25m / 0.5m / 1.0m / 1.5m
- Repeat 3 times for 6 sides (18 in total)

Results: No electrical or mechanical degradation observed.